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Polycrystallin silicon thin film transistors on Corning 7059 glass substrates using short time, l w-temperature processing.

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A new fabrication process for polycrystalline silicon thin film transistors on 7059 glass substrates is reported. This unique fabrication process has the advantages of short processing time and low processing temperature (<600 °C). The processing is based on the key step of using an ultrathin Pd layer, introduced to the surface of the glass prior to the deposition of an *a*-Si:H film, to reduce the crystallization time and temperature. It is also based on using an electron cyclotron resonance hydrogen plasma to reduced the passivation time. The *n*-channel TFTs produced by this new fabrication process have mobilities of 20 cm^2/V s, and off-currents of 0.5 pA/μm.

Polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have the potential for extensive applications in large area electronic devices such as flat panel displays and image sensors. In the last several years, many studies on poly-Si TFTs have concentrated on the reduction of the fabrication cost either by reducing the processing time, or by lowering the processing temperature. The latter effort is important since it can allow the usage of less expensive glass substrates. Work in this area has led to the demonstration that poly-Si TFTs can be fabricated on relatively inexpensive 7059 glass substrates using relatively low-temperature furnace annealing for crystallization.[1] However, this crystallization process was found to take longer than 75 h. Our previous work has showed that TFTs could be made on poly-Si films obtained by 700 °C/5 min rapid thermal annealing on 7059 glass substrates.[2] In this letter, we will show our latest efforts at reducing the processing time and temperature required for poly-Si TFTs. To be specific we will demonstrate for the first time that poly-Si TFTs can be made on 7059 glass using a unique 600 °C/2 h furnace crystallization process.

The structure of the *n*-channel poly-Si TFTs fabricated by this unique processing is shown in Fig. 1. The key step in achieving our low temperature, short time processing for these TFTs involves the deposition of the ultrathin Pd layer seen (not to scale) in Fig. 1. This ultrathin Pd layer is thermally evaporated on the 7059 glass substrate prior to the deposition of a precursor *a*-Si film which will become the poly-Si of the TFTs. We found that no special handling of the Pd coated samples was needed before the *a*-Si film deposition, however, samples were quickly processed and always kept in a clean room environment. The motivation for using this ultrathin Pd treatment of the glass comes from our earlier published work on lowering crystallization temperature. That previous work has already demonstrated that ultrathin Pd layer treatments on the surface of plasma enhanced chemical vapor deposited (PECVD) *a*-Si:H films allowed these films to be crystallized at a temperature more than 50 °C lower than films without this Pd layer for the same annealing time.[3] However, no TFTs were made with these films since the Pd-layer treatment went to the upper surface where the channel would be. In this study we use the Pd-layer treatment, but for the first time at what will be the poly-Si/glass interface. We report for the first time on transistors made with films using this unique temperature-lowering approach. We find for the annealing temperature of 600 °C that it takes 15 h to crystallize our PECVD *a*-Si:H films without this Pd layer treatment of the glass substrate and it only takes 2 h to crystallize the same *a*-Si:H with the Pd layer treatment. We find that this 600 °C/2 h processing yields the best low-temperature short time processing TFT characteristics yet reported on 7059 glass substrates.

The unique feature of the work reported here, as already pointed out, is the use of Pd-treated films in TFT fabrication and, in particular, the use of an ultrathin Pd film is deposited on the glass substrate prior to the PECVD *a*-Si films. The Pd layers used were nominally (as measured by a crystal thickness monitor) <10 Å. Obviously, such layers are not continuous films but are composed of isolated Pd islands on the 7059 glass substrates. These islands become nucleation enhancing sites for the subsequently deposited *a*-Si films and thereby reduce the crystallization temperature-time requirements.[3]

After the Pd ultrathin film is deposited on the 7059 glass, a 1000 Å PECVD *a*-Si:H film was deposited. The base pressure and the processing pressure were 5×10^{-7} and 0.5 Torr, respectively, during the PECVD step. The rf power was 200 mW/cm^2. After the *a*-Si:H deposition, the source and drain regions of these TFTs were defined and implanted with 2×10^{15} cm^{-2} phosphorus at 35 keV. It is at this point that the samples are annealed at 600 °C for 2 h to crystallize the *a*-Si films and to activate the dopants.

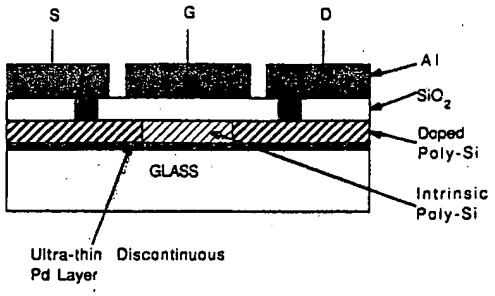

FIG. 1. Structure of the TFTs fabricated in this study.

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After this annealing, the source/drain sheet resistance reached 5 KΩ/□, which was below the range where it could limit the on-current. Neither peel off nor cracks were found on the crystallized films under an optical microscope. The size of the glass substrates was 1.5×1.5 in. and no substrate warpage was observed on these samples. However, the lateral shrinkage of these 7059 glass substrates was about 0.1% after this annealing. One can use a glass preannealing to avoid this shrinking for larger area devices. For the same annealing conditions, 2 h at 600 °C, the PECVD *a*-Si:H films without the ultrathin Pd layer did not crystallize and still kept their amorphous structure as noted from TEM observations.[3]

A 1000 Å silicon dioxide was then deposited by the same magnetron sputtering technique we have used in our earlier processing.[2] This deposition procedure uses sputtering of a SiO_2 target in an Ar/O_2 ambient to form the gate dielectric. The base pressure and processing pressure were 10^{-7} and 3×10^{-3} Torr, respectively. The samples were held at 400 °C during the deposition. Finally, the contact windows were opened by wet etching, and 1 μm Al film was thermally evaporated to form the source, drain and gate contacts. The TFTs fabricated in this study had a channel length of 7.5 μm and a channel width of 75 μm.

After the TFT structure was completed, the TFTs were passivated using an electron cyclotron resonance (ECR) hydrogen plasma. In our previous work,[4,5] we have shown that this ECR hydrogenation is a very effective passivation technique that can reduce the passivation time (the minimum processing time to reach the optimum TFT performance) from several hours, which is usually required by rf plasma hydrogenation, to times of the order of 10 min. We believe that the reduction in passivation time is attributable to higher H and H^+ concentrations in the ECR plasma compared to a rf plasma.[4,5] The base pressure and processing pressure for our ECR hydrogenation used in this study were 1×10^{-6} and 1.4×10^{-4} Torr, respectively. The microwave power was 600 W and the substrate temperature was 300 °C during the passivation. In this study, the TFTs were passivated using the ECR hydrogen plasma for 10 min.

Figure 2 shows the output characteristics of these TFTs fabricated as described above. The effective mobility of these devices, calculated in the linear region at maximum transconductance, was 20 cm^2/V s. When the same fabrication process was followed but without the use of the ultrathin Pd layer, the resulting TFTs had corresponding mobilities that were less than 1 cm^2/V s. Again, this is due to the fact that, without the ultrathin Pd layer, the PECVD *a*-Si:H films would not crystallize after a 600 °C/2 h annealing. The subthreshold characteristics are shown in Fig. 3. The inverse subthreshold slope of these TFTs was 1.3 V/decade for drain bias of 5 V. We believe that a high interface state density at the Si/SiO_2 interface is responsible for this relatively high inverse subthreshold slope. The interface state density calculated from the trapping model[6] was 9×10^{11} cm^{-2}. The threshold voltage was 2 V where we defined this threshold voltage as the gate bias at which the normalized drain current I_{dn} [$I_{dn}=I_d/(W/L)$] equals

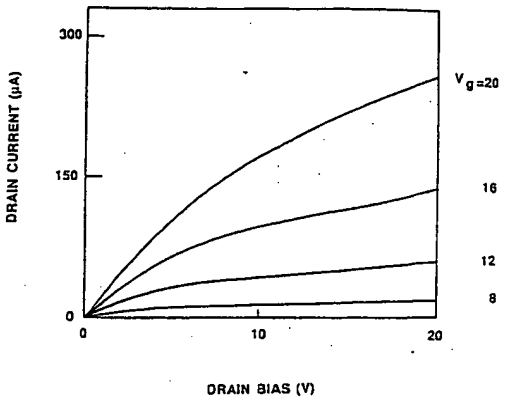

FIG. 2. Output characteristics of the poly-Si TFTs with an ultrathin Pd layer.

10^{-7} A. Here W is the channel width and L is the channel length. We have found that TFTs with the ECR hydrogenation used here usually have a lower threshold voltage than the same TFTs with a rf hydrogenation.

Since the off current is often a function of the gate voltage in TFTs, it is convenient to define a minimum off-current as the minimum drain current for gate voltages ≤0 V with a drain bias of 5 V. As shown in Fig. 3, the minimum off-current for these TFTs was in the 10^{-11} A range for a channel width of 75 μm, which gives a minimum off-current per unit gate width of 0.5 pA/μm. We defined an on/off current ratio between the maximum forward current, and the minimum off-current for a gate voltage ranging from −20 to 20 V and a drain bias of 5 V. With this condition the on/off current ratio of these TFTs was in the 10^6 range. We note that this is for TFT structures fabricated using temperatures that did not exceed 600 °C at any stage during the whole processing sequence.

In conclusion, we have for the first time demonstrated an *n*-channel poly-Si TFT fabrication process that uses a unique Pd-assisted 600 °C crystallization step and an ECR

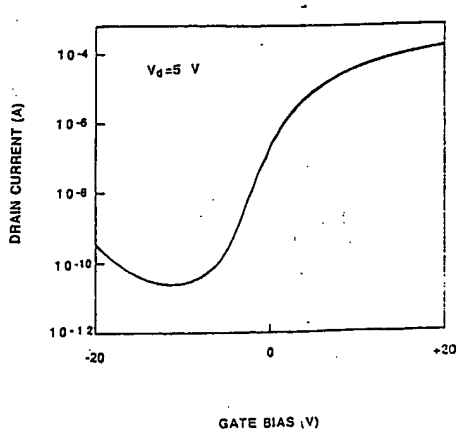

FIG. 3. Subthreshold characteristics of the poly-Si TFTs with an ultrathin Pd layer.

plasma passivation step. This new fabrication process has the advantages of short processing time and low processing temperature. We found that the ultrathin Pd layer treatment of the 7059 glass substrate can reduce the crystallization time for the PECVD a-Si:H films at 600 °C from 15 to 2 h. In addition, the usage of the ECR passivation technique can reduce the passivation time to 10 min compared to several hours when using a conventional rf plasma passivation. The reduction in processing time resulting from this unique fabrication process can benefit the mass production of TFTs, and the maximum processing temperature of 600 °C is compatible with the use of the relatively inexpensive 7059 glass substrates. The poly-Si TFTs fabricated on 7059 glass substrates using the process described above had a effective mobility of 20 cm^2/V s, a threshold voltage of 2 V, a minimum off current of 0.5 $pA/\mu m$ at a drain bias of 5 V, and an on/off current ratio of 10^6 at a drain bias of 5 V.

The authors wish to thank Dr. Somnath Nag for depositing the PECVD a-Si:H films used in this work. We also wish to thank 3M Corporation, Sarnoff Research Labs, and Kurt J. Lesker Co. for their support of this research.

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